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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,081	03/23/2004	Hung-Wei Chen	TS03-627	3848
42717	7590	09/23/2005	EXAMINER	
HAYNES AND BOONE, LLP 901 MAIN STREET, SUITE 3100 DALLAS, TX 75202			SARKAR, ASOK K	
			ART UNIT	PAPER NUMBER
			2891	

DATE MAILED: 09/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/807,081	<b>Applicant(s)</b> CHEN ET AL.	
	<b>Examiner</b> Asok K. Sarkar	<b>Art Unit</b> 2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 September 2005.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18, 20-25, 27, 28 and 30-32 is/are pending in the application.
- 4a) Of the above claim(s) 15-18, 20-25, 27, 28 and 30-32 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☒ Claim(s) 13 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>5/6/04</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election of Species I claims 1 – 14 in the reply filed on September 12, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).
2. Claims 15 – 18, 20 – 25, 27 – 28 and 30 – 32 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species II claims, there being no allowable generic or linking claim. Election was treated as being made **without** traverse in the reply filed on September 12, 2005.

### *Claim Objections*

3. Claim 13 is objected to because of the following informalities: The claim should depend on claim 12. Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

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2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1 – 10 and 12 – 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal, US 2003/0132428 in view of Ahn, US 2002/0022308 and Huang, US 6,323,106.

Regarding claim 1, Agarwal teaches method of reducing boron segregation phenomena in an N channel, metal oxide semiconductor (NMOS) device via formation of a doped insulator region formed in an underlying insulator layer, comprising the steps of:

- forming a semiconductor layer on an underlying insulator layer, wherein said insulator overlays a semiconductor substrate since he teaches SOI wafer in paragraph 23;
- forming a hard mask layer 114 and 116 on said semiconductor layer 120 (see Fig. 1A);

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- defining openings in said hard mask layer and in said semiconductor layer and creating composite stacks comprised of hard mask shapes on semiconductor shapes (see Fig. 1A);
- laterally removing portions of said hard mask shapes exposing top portions of edges of said semiconductor shapes (see Fig. 2) in paragraph 31;
- performing an ion implantation procedure to place ions in portions of said openings, and to place ions in portions of said semiconductor shapes (see Fig. 3) in paragraphs 36 – 40;
- filling said openings with a second insulator layer 616 (see Fig. 6A); and
- removing said hard mask shapes in paragraph 45.

Agarwal fails to teach the following elements: (1) exposing a portion of the insulator layer while etching the hard mask layer; (2) implanting ions in portions of said insulator layer exposed in said openings, and to place ions in portions of said insulator layer underlying portions of said semiconductor shapes and (3) performing an anneal procedure to activate said ions and forming said doped insulator region in portions of said insulator layer.

Regarding element (1), Ahn teaches forming an STI opening in an SOI substrate exposing a portion of the insulator layer while etching the hard mask layer with reference to Fig. 1 which is a well – known practice in the semiconductor industry for SOI wafers.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Agarwal and form an STI opening in an SOI substrate

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exposing a portion of the insulator layer, which is a well – known practice in the semiconductor industry for SOI wafers as taught by Ahn with reference to Fig. 1.

Regarding elements (2) and (3), Huang teaches nitrogen implantation into the oxide layers in the STI trenches so that ions are implanted in portions of the insulator layer exposed in said openings, and also in portions of said insulator layer underlying portions of said semiconductor shapes with respect to Fig. 3C and performing an anneal procedure to activate said ions and forming said doped insulator region in portions of said insulator layer in column 6, lines 25 – 37 for the benefit of reducing boron diffusion and suppress RNCE in column 4, lines 41 – 53.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Agarwal and implant ions into the oxide layers in the STI trenches so that ions are implanted in portions of the insulator layer exposed in said openings, and also in portions of said insulator layer underlying portions of said semiconductor and performing an anneal procedure to activate said ions and forming said doped insulator region in portions of said insulator layer for the benefit of reducing boron diffusion and suppress RNCE as taught by Huang in column 4, lines 41 – 53.

Regarding claims 2 – 4, Agarwal teaches the nitride layer thickness between 100 – 1500 angstroms in paragraph 25 and Huang teaches nitride deposition by PECVD in column 5, lines 46 – 50. Agarwal in view of Ahn and Huang fails to teach the thickness of the silicon and the silicon oxide insulator layer.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to judiciously adjust and control these parameters during the

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formation of the SOI wafer and implantation process through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) and it would not yield any unexpected results.

Note that the specification contains no disclosure of either the critical nature of the claimed processes or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen methods or upon another variable recited in a claim, the Applicant must show that the chosen methods or variables are critical (*Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir., 1990)). See also *In re Aller, Lacey and Hall* (10 USPQ 233 – 237).

Regarding Claim 5, Agarwal teaches etching via anisotropic RIE procedure in paragraphs 28 – 30.

Regarding Claim 6, Agarwal teaches width of the hard mask shapes is between 0.05 and 10 micron in paragraph 25.

Regarding Claim 7, Agarwal teaches pull back of masks via isotropic etch with phosphoric acid in paragraph 34.

Regarding Claim 8, Agarwal teaches lateral pull back of mask shape is between 10 – 500 angstroms in paragraph 31.

Regarding Claim 9, Agarwal teaches ion implantation procedure is performed using boron ions at an energy between about 1 to 10 KeV, at a dose between about  $1E12$  to  $1E16$  atoms/cm<sup>2</sup> and featuring an implantation angle between about 0 to 45° in paragraphs 37 – 39.

Regarding Claim 12, Agarwal in view of Huang teaches the doped insulator region is a nitrogen doped region.

Regarding Claim 14, Agarwal teaches second insulator deposited by HDPCVD in paragraph 45.

Regarding Claim 12, Huang teaches the ion implantation procedure is performed using nitrogen ions at an energy between about 1 to 10 KeV, at a dose between about  $1E12$  to  $1E16$  atoms/cm<sup>2</sup> and featuring an implantation angle between about 0 to 45° in column 6, lines 37 – 57.

Regarding claim 13, Agarwal in view of Ahn and Huang fails to teach forming the nitrogen profile below the boron profile.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Agarwal in view of Ahn and Huang and when both boron and nitrogen are used to prevent reverse narrow channel effects nitrogen profile should be formed below the boron profile because the nitrogen profile will prevent the diffusion of boron into the channel regions of neighboring transistors.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal, US 2003/0132428 in view of Ahn, US 2002/0022308 and Huang, US 6,323,106 as applied to claim 1 above, and further in view of Xiang, US 6,410,938.

Agarwal in view of Ahn and Huang fails to teach annealing to active the ions after the implantation although it is a common practice after implantation.

Xiang teaches an annealing procedure after nitrogen implant for the benefit of forming the buried nitrided oxide layer in column 4, lines 56.



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Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Agarwal in view of Ahn and Huang and anneal after the implant for the benefit of forming the buried nitrided oxide layer as taught by Xiang in column 4, lines 56. It would have been obvious to one with ordinary skill in the art at the time of the invention to anneal under low pressure hydrogen ambient to prevent the natural oxidation of the silicon that is used as the semiconductor layer.

### ***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, reading "Asok K. Sarkar". The signature is fluid and cursive, with the first name "Asok" and last name "Sarkar" clearly legible.

Asok K. Sarkar  
September 20, 2005

Primary Examiner